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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/987,563	11/15/2001	Mitsuya Kinoshita	57454-263	7536

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EXAMINER	
TRIMMINGS, JOHN P	
ART UNIT	**PAPER NUMBER**
2133	3

DATE MAILED: 03/31/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/987,563	KINOSHITA ET AL.	
	Examiner	Art Unit	
	John P Trimmings	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 November 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 November 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-12 are presented for examination.

Priority

The examiner acknowledges the applicant's foreign priority date of 3/5/2001.

Information Disclosure Statement

The examiner has considered the references of the applicant's Information Disclosure Statement.

Drawings

1. The drawings are objected to because FIG.1 MEMORY ARRAY 10 contains the data line "G1010", but the examiner believes it should instead be "G101". A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

2. The disclosure is objected to because of the following informalities: page 10 line 14 recites, "...loads of the two EXOR...", but the examiner believes it should read, "...loads of two EXOR...". Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 7 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The examiner notes that line 7 of the claim receives "a corresponding data bit", and in line 9 establishes the corresponding data as "teacher bit", but then in line 10 compares the "teacher" and "corresponding data bit" together. The applicant is therefore comparing the same bit to itself, and so it is indefinite in the eyes of the examiner as to exactly what bits are being compared.

4. Claim 9 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The claim states that the data are coupled to a number of 1st circuits that is equal to the number of 1st circuits. The claim is indefinite because the examiner is unsure as to the meaning of this claim, where the number of 1st circuits can be anything because it depends upon the number of the same 1st circuits.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-4, 6-9 and 11-12 are rejected under 35 U.S.C. 102(b) as being anticipated by McClure et al., U.S. Patent No. 5311473.

As per Claim 1:

McClure et al. teaches a multi-bit test circuit for determining a match in logical level among a plurality of data bits read out in parallel from a memory array (see Abstract), comprising: a plurality of first determining circuits (FIG.3 50_0 or 50_1), arranged corresponding to said plurality of data bits (64 bits in the example of FIG.2), each for receiving, as a pair, a corresponding data bit and a teacher data bit placed in a predetermined relation with said corresponding data bit in the plurality of data bits (bit for bit as in FIG.4 60), and determining a match in logical level between received data bits FIG.4 60, 62, 64, 68), data bits in each pair including different teacher data bits from other pair(s) (FIG.4 18_0 , 18_1), and a final determining circuit for outputting a final determination signal indicating a match in logical level among said plurality of data bits in accordance with output signals of said plurality of first determining circuits (FIG.3 58, 59).

As per Claim 2:

McClure et al. teaches the multi-bit test circuit according to claim 1, wherein said plurality of data bits are divided into a plurality of groups (FIG.1 12_0 to 12_7), each having a predetermined number of data bits (FIG.1 18, 8 bits), and each of said plurality of first determining circuits (FIG.4 50_0) receives, as a teacher data bit thereof, a data bit in a different group from a corresponding group including a corresponding data bit and in a same position in the different group as a position of the corresponding data bit in the corresponding group (FIG.4 group 18_0 bits 0-7 and group 18_1 bits 0-7).

As per Claims 3 and 7:

McClure et al. teaches the multi-bit test circuit according to claim 1, wherein said plurality of data bits are applied in parallel (FIG.2 PARALLEL TEST CIRCUITRY 28), and divided into a plurality of groups (FIG.1 12_0 to 12_7) each having a same data width (FIG.1 18, 8 bits), and each of said plurality of first determining circuits (FIG.3 50_0 to 50_3) receives, as said teacher data bit, a data bit that is in a group adjacent to a corresponding group including a corresponding data bit and in a corresponding position in the adjacent group to a position of the corresponding data bit in the corresponding group (FIG.4 group 18_0 bits 0-7 and adjacent group 18_1 bits 0-7).

As per Claim 4:

McClure et al. teaches the multi-bit test circuit according to claim 3, wherein said plurality of first determining circuits (FIG.3 50_0 to 50_3) is smaller in number (4) than said plurality of data bits (FIG.3 18_0 to 18_7 times 8 = 64 bits).

As per Claim 6:

McClure et al. teaches the multi-bit test circuit according to claim 1, wherein said plurality of data bits are applied in parallel (FIG.2 PARALLEL TEST CIRCUITRY 28), and divided into a plurality of groups (FIG.1 12_0 to 12_7) having a same bit width (FIG.1 18, 8 bits); and said plurality of first determining circuits (FIG.3 50_0 to 50_3) are arranged corresponding to said plurality of data bits (bits 0-63 are distributed to these circuits in order of 18_0 to 18_7) respectively, and receive, as teacher data bits, data bits in corresponding positions, in groups different from the groups of corresponding data bits (FIG.4 group 18_0 bits 0-7 and adjacent group 18_1 bits 0-7).

As per Claim 8:

McClure et al. teaches the multi-bit test circuit according to claim 1, further comprising a teacher signal transmission bus for transmitting expected value teacher data of plural bits (for example, FIG.3 18_1), wherein said plurality of data bits are applied in parallel (FIG.2 PARALLEL TEST CIRCUITRY 28), and divided into a plurality of groups (FIG.1 12_0 to 12_7) each having a predetermined number of data bits (FIG.1 18, 8 bits); and said teacher signal transmission bus has a same bit width as the groups of the data bits, and said plurality of first determining circuits comprises: a plurality of first determination gates (FIG.4 60), arranged corresponding to respective data bits in a predetermined number of groups of said plurality of groups of data bits (FIG.4 18_0 bits 0-7), each receiving a corresponding data bit and a data bit in a corresponding position in a group different from a group including the corresponding data bit as said teacher data bits (FIG.4 18_1 bits 0-7) and a plurality of second determination gates (FIG.3 54L

and FIG.4 61), arranged corresponding to the respective data bits in other groups (FIG.4 18_2 bits 0-7), each receiving a corresponding data bit in a corresponding group (FIG.5 18_1)and a corresponding expected value teacher data bit of said expected value teacher data of plural bits (FIG.4 18_2 bits 0-7).

As per Claim 9:

McClure et al. teaches The multi-bit test circuit according to claim 1, wherein the data bits each are coupled to a same number of first determining circuits of said plurality of first determination circuits (FIG.3 shows 4 circuits).

As per Claim 11:

McClure et al. teaches a multi-bit test circuit (see Abstract) comprising: a plurality of data lines for selecting plurality of data bits (FIG.1 A7-A16), said plurality of data bits being divided into at least three groups (FIG1 12_0 - 12_7) having a same bit width (FIG1 18 is 8 bits); a plurality of determination gates (FIG3 50_0 - 50_3), arranged corresponding to said plurality of data lines, each receiving, as teacher data, a data bit in a different group from a corresponding group (FIG.4 18_1) and determining a match in logical level between a data bit of a corresponding data line (FIG.4 18_0) and received teacher data (FIG.4 18_1); and a final determination circuit for generating a signal indicating a match in logical level among said plurality of data bits in accordance with output signals of said plurality of determination gates (FIG.3 58, 59).

As per Claim 12:

McClure et al. teaches The multi-bit test circuit according to claim 11, wherein said teacher data is located in a same position in the different group

as a position of the corresponding data bit in the corresponding group (example; FIG.4 data = 18_0 <0> and teacher = 18_1 <0>).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of

35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over McClure et al., U.S. Patent No. 5311473 as applied to claim 3 above, and in view of Toshiya Uchida, U.S. Patent No. 5579272. McClure et al. teaches the multi-bit test circuit according to claim 3, wherein each of said plurality of first determining circuits (FIG.3 50_0 to 50_3) receives, as said teacher data bit, a data bit in a corresponding position, to a position of a corresponding data bit, in a group adjacent (FIG.4 18_1 <0> for example), but fails to teach the receiving of the bits in a cyclic manner among said plurality of groups. However, in an analogous art, Uchida shows this arrangement in FIG.1, where each determining circuit (FIG.1 40) equally shares in teaching bits (FIG.1 D0 for example) from adjacent groups (FIG.1 10, 11, 12, 13). And Uchida, in column 3 lines 7-13, recites the advantage as a better data compression method (cyclic), which allows for more diverse testing algorithms. And one with ordinary skill in the art at the time of the invention, motivated as suggested by Uchida, would combine the two references, and so the claim is rejected.

8. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over McClure et al., U.S. Patent No. 5311473 as applied to claim 1 above, and in view of Tomishima et al., U.S. Patent No. 5838627. McClure et al. fails to teach setting data interconnection lines so that circuit loading is substantially the same. However, in an analogous art, Tomishima et al. teaches designing data lines of

equal length (column 4 lines 36-45) in relation to the data path. And Tomishima et al., in column 5 lines 1-7 establishes the advantage to the invention as giving the user better data timing margins and high-speed access. And one with ordinary skill in the art at the time of the invention, motivated as suggested by Tomishima et al., would combine the two references, and so the claim is rejected.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John P Trimmings whose telephone number is 703-305-0714. The examiner can normally be reached on Mondat through Thursday, 7:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on 703-305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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